IN THE CLAIMS:

Please CANCEL claims 1, 14, and 27, without prejudice or disclaimer, as shown below.

Please ADD claim 33 as shown below.

Please AMEND claims 2-8, 10, 12-13, 15-21, 23, 25-26, 28, and 30-32 as shown below.

1. (Cancelled)

2. (Currently Amended) A network switch as recited in claim ~~1~~8, wherein each set of said at least two sets of communication channels comprises three communication channels.

3. (Currently Amended) A network switch for network communications, said network switch comprising:

a first data port interface, said first data port interface supporting at least one data port transmitting and receiving data;

a second data port interface, said second data port interface supporting at least one data port transmitting and receiving data;

a CPU interface, said CPU interface configured to communicate with a CPU;

a common memory, said common memory communicating with said first data port interface and said second data port interface;

a memory management unit, said memory management unit for communicating data from said first data port interface and said second data port interface and said common memory; and

at least two sets of communication channels, with each of said communication channels communicating data and messaging information between said first data port interface, said second data port interface, and said memory management unit,

wherein one set of communication channels of the at least two sets of communication channels provides communication from said first and second data port interfaces to said memory management unit and another set of communication channels of the at least two sets of communication channels provides communication from said memory management unit to said first and second data port interfaces,

wherein the first data port interface, the second data port interface, the CPU interface, the common memory, the memory management unit and the at least two sets of communication channels are embodied on a single substrate,

wherein each set of said at least two sets of communication channels comprises three communication channels, and

~~A network switch as recited in claim 2,~~ wherein said three communication channels include a first channel for communicating cell data between data ports of the first data port interface, data ports of the second data port interface, and the common

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memory, a second channel, synchronously locked with the first channel, for communicating message information corresponding to the cell data on the first channel, and a third channel, shared between the sets of communication channels, independent from said first and second channel, for communicating sideband message information.

4. (Currently Amended) A network switch as recited in claim ~~1~~8, wherein at least one of said first and second data port interfaces is a gigabit data port interface.

5. (Currently Amended) A network switch as recited in claim ~~1~~8, wherein said first data port interface, said second data port interface, said CPU interface, said common memory, said memory management unit, and said at least two sets of communication channels are integrated on a single application specific integrated circuit (ASIC) chip.

6. (Currently Amended) A network switch as recited in claim ~~1~~8, wherein said first data port interface, said second data port interface, said CPU interface, said common memory, said memory management unit, and said at least two sets of communication channels are configured to perform layer two switching at wirespeed.

7. (Currently Amended) A network switch as recited in claim ~~1~~8, wherein said first data port interface, said second data port interface, said CPU interface, said common memory, said memory management unit, and said at least two sets of communication channels are configured to perform layer three switching at wirespeed.

8. (Currently Amended) A network switch for network communications, said network switch comprising:

a first data port interface, said first data port interface supporting at least one data port transmitting and receiving data;

a second data port interface, said second data port interface supporting at least one data port transmitting and receiving data;

a CPU interface, said CPU interface configured to communicate with a CPU;

a common memory, said common memory communicating with said first data port interface and said second data port interface;

a memory management unit, said memory management unit for communicating data from said first data port interface and said second data port interface and said common memory; and

at least two sets of communication channels, with each of said communication channels communicating data and messaging information between said first data port interface, said second data port interface, and said memory management unit,

wherein one set of communication channels of the at least two sets of communication channels provides communication from said first and second data port interfaces to said memory management unit and another set of communication channels of the at least two sets of communication channels provides communication from said memory management unit to said first and second data port interfaces,

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wherein the first data port interface, the second data port interface, the CPU

interface, the common memory, the memory management unit and the at least two sets of

communication channels are embodied on a single substrate, and

~~A network switch as recited in claim 1,~~ wherein said CPU interface is configured

to provide communication between a remote CPU and the at least two sets of

communication channels, wherein said remote CPU can program operations of the

memory management unit while one of the first and second data port interfaces are

receiving or transmitting data.

9. (Original) A network switch as recited in claim 8, wherein said CPU interface

is configured to provide communication between the remote CPU and a sideband channel

of the at least two sets of communication channels.

10. (Currently Amended) A network switch as recited in claim ~~1~~8, said network

switch including a plurality of semiconductor-implemented lookup tables therein, said

plurality of lookup tables including address resolution lookup/layer three lookup, rules

tables, and VLAN tables.

11. (Original) A network switch as recited in claim 10, wherein said first data port

interface communicates table information with said second data port interface, such that

incoming address information can be updated at a plurality of data port interfaces while

the information is received at one data port interface.

12. (Currently Amended) A network switch as recited in claim ~~1~~8, wherein said first data port interface includes an auto-negotiating unit for negotiating a maximum communication speed between a source data port and a destination data port.

13. (Currently Amended) <u>A network switch for network communications, said network switch comprising:</u>

<u>a first data port interface, said first data port interface supporting at least one data port transmitting and receiving data;</u>

<u>a second data port interface, said second data port interface supporting at least one data port transmitting and receiving data;</u>

<u>a CPU interface, said CPU interface configured to communicate with a CPU;</u>

<u>a common memory, said common memory communicating with said first data port interface and said second data port interface;</u>

<u>a memory management unit, said memory management unit for communicating data from said first data port interface and said second data port interface and said common memory; and</u>

<u>at least two sets of communication channels, with each of said communication channels communicating data and messaging information between said first data port interface, said second data port interface, and said memory management unit,</u>

<u>wherein one set of communication channels of the at least two sets of communication channels provides communication from said first and second data port</u>

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interfaces to said memory management unit and another set of communication channels of the at least two sets of communication channels provides communication from said memory management unit to said first and second data port interfaces,

wherein the first data port interface, the second data port interface, the CPU interface, the common memory, the memory management unit and the at least two sets of communication channels are embodied on a single substrate,

said network switch including a plurality of semiconductor-implemented lookup tables therein, said plurality of lookup tables including address resolution lookup/layer three lookup, rules tables, and VLAN tables, and

A network switch as recited in claim 10, wherein said first data port interface and said second data port interface share a common address lookup/layer three table, and a common VLAN table, and wherein each of the first data port interface and the second data port interface has a unique rules table associated therewith.

14. (Cancelled)

15. (Currently Amended) A network switch as recited in claim ~~14~~21, wherein each set of said at least two sets of communication channel means comprises three communication channels.

16. (Currently Amended) A network switch for network communications, said network switch comprising:

first data means providing a first data port interface supporting at least one data port transmitting and receiving data;

second data means providing a second data port interface supporting at least one data port transmitting and receiving data;

interface means providing an interface configured to communicate with a CPU;

means for storing data, said means for storing data communicating with said first data means and said second data means;

means for managing memory, said means for managing memory communicating data from said first data means and said second data means and said means for storing data; and

at least two sets of communication channel means, with each of said communication channel means communicating data and messaging information between said first data means, said second data means, and said means for managing memory,

wherein one set of communication channel means of the at least two sets of communication channel means provides communication from said first and second data means to said means for managing memory and another set of communication channel means of the at least two sets of communication channel means provides communication from said means for managing memory to said first and second data means,

wherein the first data means, the second data means, the interface means, the means for storing data, the means for managing memory and the at least two sets of communication channel means are embodied on a single substrate,

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wherein each set of said at least two sets of communication channel means

comprises three communication channels, and

A network switch as recited in claim 15, wherein said three communication

channels include a first channel for communicating cell data between data ports of the

first data port interface, data ports of the second data port interface, and the means for

storing data, a second channel, synchronously locked with the first channel, for

communicating message information corresponding to the cell data on the first channel,

and a third channel, shared between the sets of communication channels, independent

from said first and second channel, for communicating sideband message information.

17. (Currently Amended) A network switch as recited in claim 1421, wherein at

least one of said first and second data means is a gigabit data port interface.

18. (Currently Amended) A network switch as recited in claim 1421, wherein said

first data means, said second data means, said interface means, said means for storing

data, said means for managing memory, and said at least two sets of communication

channel means are integrated on a single application specific integrated circuit (ASIC)

chip.

19. (Currently Amended) A network switch as recited in claim 1421, wherein said

first data means, said second data means, said interface means, said means for storing

data, said means for managing memory, and said at least two sets of communication channel means are configured to perform layer two switching at wirespeed.

20. (Currently Amended) A network switch as recited in claim ~~14~~21, wherein said first data means, said second data means, said interface means, said means for storing data, said means for managing memory, and said at least two sets of communication channel means are configured to perform layer three switching at wirespeed.

21. (Currently Amended) A network switch for network communications, said network switch comprising:

first data means providing a first data port interface supporting at least one data port transmitting and receiving data;

second data means providing a second data port interface supporting at least one data port transmitting and receiving data;

interface means providing an interface configured to communicate with a CPU;

means for storing data, said means for storing data communicating with said first data means and said second data means;

means for managing memory, said means for managing memory communicating data from said first data means and said second data means and said means for storing data; and

at least two sets of communication channel means, with each of said communication channel means communicating data and messaging information between said first data means, said second data means, and said means for managing memory,

wherein one set of communication channel means of the at least two sets of communication channel means provides communication from said first and second data means to said means for managing memory and another set of communication channel means of the at least two sets of communication channel means provides communication from said means for managing memory to said first and second data means,

wherein the first data means, the second data means, the interface means, the means for storing data, the means for managing memory and the at least two sets of communication channel means are embodied on a single substrate, and

~~A network switch as recited in claim 14,~~ wherein said interface means is configured to provide communication between a remote CPU and the at least two sets of communication channel means, wherein said remote CPU can program operations of the means for managing memory while one of the first and second data means are receiving or transmitting data.

22. (Original) A network switch as recited in claim 21, wherein said interface means is configured to provide communication between the remote CPU and a sideband channel of the at least two sets of communication channel means.

23. (Currently Amended) A network switch as recited in claim ~~14~~21, said network switch including a plurality of semiconductor-implemented lookup tables therein, said plurality of lookup tables including address resolution lookup/layer three lookup, rules tables, and VLAN tables.

24. (Original) A network switch as recited in claim 23, wherein said first data means communicates table information with said second data means, such that incoming address information can be updated at a plurality of data port means while the information is received at one data means.

25. (Currently Amended) A network switch as recited in claim ~~14~~21, wherein said first data means includes an auto-negotiating means for negotiating a maximum communication speed between a source data port and a destination data port.

26. (Currently Amended) A network switch for network communications, said network switch comprising:

first data means providing a first data port interface supporting at least one data port transmitting and receiving data;

second data means providing a second data port interface supporting at least one data port transmitting and receiving data;

interface means providing an interface configured to communicate with a CPU;

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means for storing data, said means for storing data communicating with said first data means and said second data means;

means for managing memory, said means for managing memory communicating data from said first data means and said second data means and said means for storing data; and

at least two sets of communication channel means, with each of said communication channel means communicating data and messaging information between said first data means, said second data means, and said means for managing memory,

wherein one set of communication channel means of the at least two sets of communication channel means provides communication from said first and second data means to said means for managing memory and another set of communication channel means of the at least two sets of communication channel means provides communication from said means for managing memory to said first and second data means,

wherein the first data means, the second data means, the interface means, the means for storing data, the means for managing memory and the at least two sets of communication channel means are embodied on a single substrate,

wherein said network switch comprises a plurality of semiconductor-implemented lookup tables therein, said plurality of lookup tables including address resolution lookup/layer three lookup, rules tables, and VLAN tables, and

~~A network switch as recited in claim 23,~~ wherein said first data means and said second data means share a common address lookup/layer three table, and a common

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VLAN table, and wherein each of the first data means and the second data means has a unique rules table associated therewith.

27. (Cancelled)

28. (Currently Amended) A method of handling data packets in a network switch, said method comprising the steps of:

receiving at a data port an incoming data packet;

resolving a destination address of said incoming data packet;

discarding, forwarding, or modifying the packet based upon the resolving step;

placing at least a portion of said data packet on a first communication channel, when the packet is to be forwarded,

receiving at said data port a section of another data packet on a second communication channel from a common memory; and

forwarding said another data packet from said data port;

wherein said first and second channels are separate from each other,

wherein the steps are performed in a single network switch on a single substrate with the common memory,

A method of handling data packets as recited in claim 27, wherein said step of placing at least a portion of said data packet on a first communication channel further includes placing an associated control message on a third communication channel, and

wherein said step of receiving at said data port a section of another data packet further comprises receiving an associated control message on a fourth communication channel from the common memory, and

wherein the first, second, third and fourth communication channels are separate but the first and third are synchronized with each other and the second and fourth are synchronized with each other.

29. (Original) A method of handling data packets as recited in claim 28, further comprising sending and receiving, by said data port, sideband message information on a fifth communication channel.

30. (Currently Amended) A method of handling data packets as recited in claim 2728, wherein said network switch performs layer two switching at wirespeed.

31. (Currently Amended) A method of handling data packets as recited in claim 2728, wherein said network switch performs layer three switching at wirespeed.

32. (Currently Amended) A network switch as recited in claim 2728, wherein said network switch has a plurality of data ports, and wherein said step of resolving a destination address of said incoming data packet further comprises updating address information used in forwarding data packets at said plurality of data ports while the address information is received at one data port of said plurality of data ports.

33. (New) A method of handling data packets in a network switch, said method comprising the steps of:

receiving at a data port an incoming data packet;

resolving a destination address of said incoming data packet;

discarding, forwarding, or modifying the packet based upon the resolving step;

placing at least a portion of said data packet on a first communication channel, when the packet is to be forwarded,

receiving at said data port a section of another data packet on a second communication channel from a common memory; and

forwarding said another data packet from said data port;

wherein said first and second channels are separate from each other and said first channel is synchronized to a third channel that is separate from the first channel and the second channel, and

wherein the steps are performed in a single network switch on a single substrate with the common memory.